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Design of High Speed Multiplier using Vedic Mathematics

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Abstract— With the advancement of technology, a processor is required to have high speed. Multiplication is a critical operation of Digital Signal processing(DSP) applications(like DFT, FFT, convolution etc), Arithmetic and logic unit(ALU), and Multiply and Accumulate(MAC) unit(which is basically a multiplier itself). High Speed Multiplication is thus an essential requirement to increase the performance of processor.

In this paper, we are presenting a multiplier, in which the basic multiplication is performed using one of the techniques of Vedic Mathematics, and the accumulation of partial products is done using a specific design. Both the design and the vedic technique, results in a high speed multiplier. Vedic Mathematics is based on 16 sutras, out of which we are using "Urdhva triyagbhyam" sutra. In this technique intermediate products are generated in parallel, that makes multiplication faster. We have synthesized our design using Xilinx ISE tool and compared its speed with "Modified Booth Wallace Multiplier", "High speed Vedic Multiplier" by Ramesh Pushpangadam and "Vedic Mathematics based Multiply Accumulate Unit" by Kabiraj Sethi. Our proposed Design seems to have better speed.

Keywords— Vedic Mathematics, Urdhav Tiryagbhyam, VLSI, Verilog, Modified Booth Wallace Multiplier, ALU, Booth Multiplier

INTRODUCTION

The speed of a processor, determines its performance. High speed processing is an essential requirement for all the systems. Multiplication is a significant operation in Digital signal processors and ALU, and thus the demand for high speed multiplication is continuously increasing in modern VLSI design. Our research focus is on high speed multiplication using Vedic Mathematics. Earlier some multipliers like booth multiplier[1], Modified Booth Multiplier[2,3], and array multipliers[4] were considered for high speed multiplication, but these multipliers involve large number of intermediate steps, which reduces their speed, with increase in the number of bits.

For high speed multiplication as well as to increase the performance of multiplier, Vedic Mathematics techniques are used[7-11]. The Sanskrit word Veda is derived from the root Vid, meaning to know without limit. Swami Bharati Krishna Tirtha, culled a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He developed methods and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics[5]. The Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations.

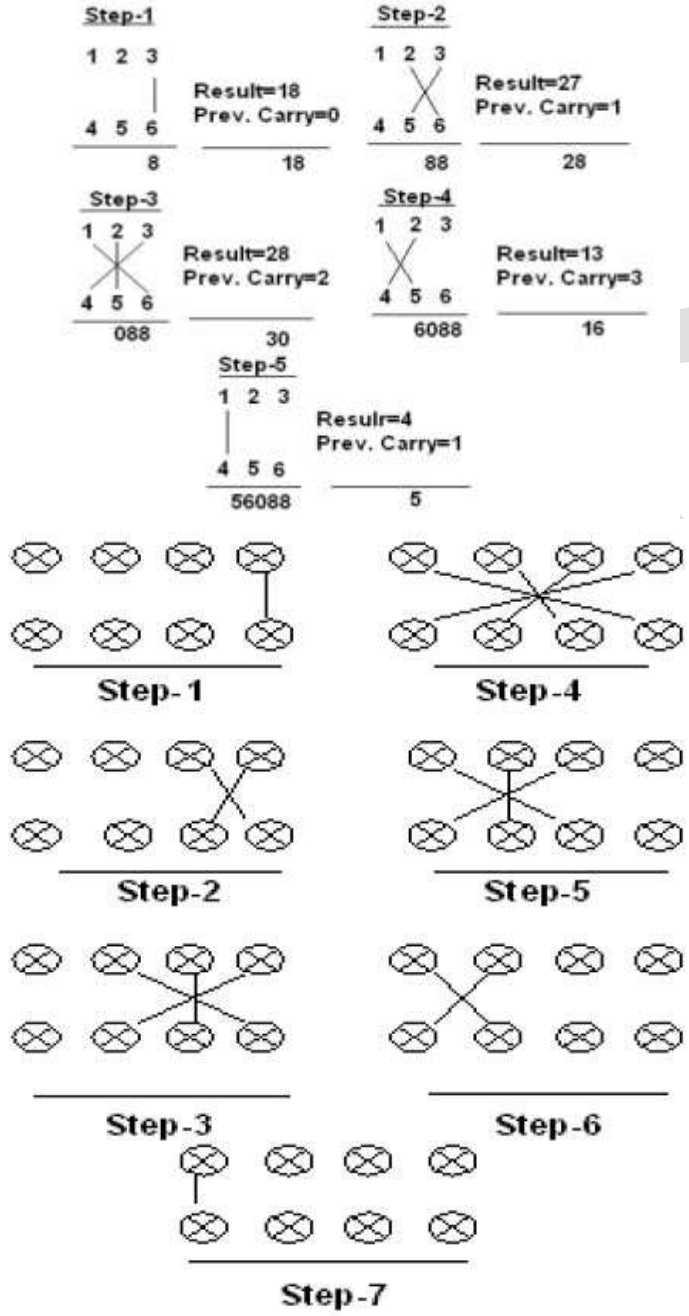
Out of these 16 sutras, our emphasis is on Urdhva Triyagbhyam technique, which is based on vertical and crosswise multiplication. Vedic mathematics is highly coherent and unified. Multiplication can be reversed to achieve one line division, squaring can be reversed to generate square root. In Vedic Mathematics partial products are generated in parallel, which increases the speed of operation[6]. In this paper we are proposing a design for accumulation of these intermediate products, with minimal delay.

Section II deals with the Urdhva Tiryagbhyam technique, which is used for basic multiplication. Section III describes basic multiplier architecture, Section IV describes our proposed design. Section V deals with results and their comparison with other multipliers and Vedic Designs.

I. VEDIC TECHNIQUE-URDHAV TIRYAGBHYAM

Among all the techniques used in Vedic Mathematics for multiplication, Urdhav Tiryagbhyam is the most preferred technique. Urdhav Tiryagbhyam means vertically and crosswise multiplication. It was discovered for fast and convenient multiplication of decimal numbers, and in our design we are using this ability for multiplication of binary numbers. The partial products are generated in parallel, which provides fast multiplication. The biggest advantage is that, it can be implemented with reduced number of AND gates, Full Adders and Half Adders.

We will first consider an example, which shows multiplication of two decimal numbers 123*456, as shown in Fig. 1. Firstly we take the product of least significant bits of the multiplier and multiplicand, the least significant bit of the result i.e. 8 in this case, is stored and carry is generated for the next step i.e. 1. In the next step, crosswise two least significant bits are multiplied, and their product is added with the previous carry. Similarly in the next step all the bits are multiplied crosswise and their products are summed up with the previous carry. Again In the next step, two most significant bits are multiplied crosswise, and results are added in the



similar manner. And finally, the most significant bit of the multiplier and multiplicand are multiplied, and result is added with the previously generated carry, to get the end result.

Fig.1. Line Diagram for multiplication of decimal numbers

We can apply this sutra in the similar manner, to binary numbers. As shown in Fig. 2, the bits of multiplier and multiplicand are multiplied crosswise. They are added with previous carry, to generate the result of that particular step. The final result is obtained by concatenating, the result from each step and the carry in the last step. For convenience bits are represented by circles in figure.

Fig.2. Line Diagram for multiplication of binary numbers

II. BASIC MULTIPLIER ARCHITECTURE

2*2 Multiplier Architecture is obtained by using 2 half adders and four and gates, as shown in Fig. 3. The product X0Y0 is directly given to the output. X1Y0 and X0Y1 are added using first half adder, sum is given directly to the output and carry is added with product X1Y1 using second half adder.

S0=X0*Y0

C1S1=X0*Y1+X1*Y0

C2S2=X1*Y1+C1

Result={C2S2S1S0}

where Sn and Cn are the sum and carry output respectively.

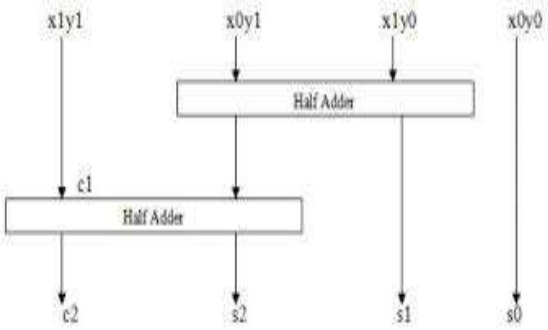


Fig.3. Architecture of 2*2 Multiplier

III. PROPOSED DESIGN

The architecture of 4*4 Multiplier consists of four 2*2 Multipliers, a 4-bit carry save adder, a 5-bit adder, and a 2-bit adder as shown in Fig. 4. This design, performs the accumulation of partial products in such a way, that it reduces the delay, compared to other multipliers, along with that partial products are generated in parallel, so delay is further reduced.

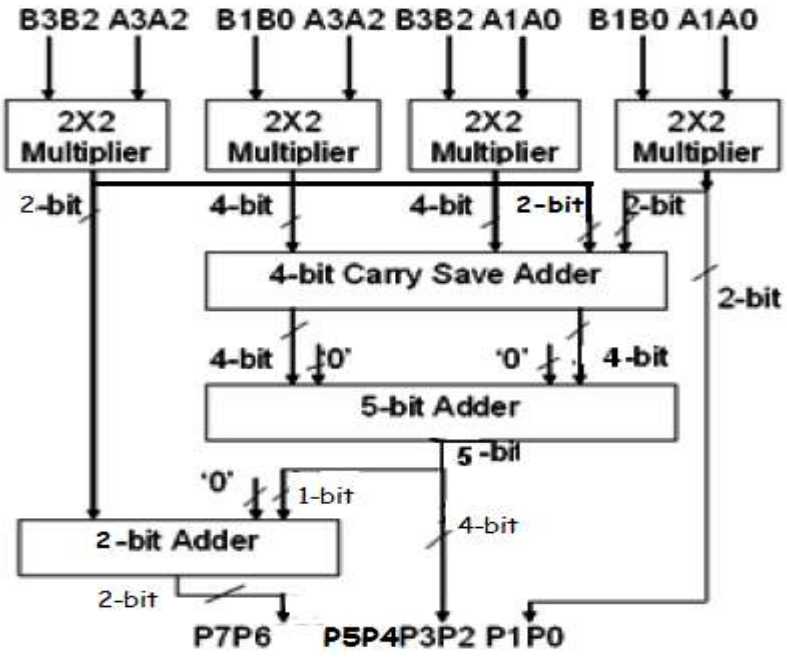


Fig.4. Architecture of 4*4 Multiplier

The least significant two bits of the first 2*2 multiplier are directly given to the output as output bits P1P0. The most significant bits of the output of the same multiplier are concatenated with the least significant two bits of the fourth multiplier, and the resulting value is added with 4-bit outputs of the second and third multiplier using carry save adder. The sum and carry output of carry save adder are added using a 5-bit adder. The least significant four bits obtained as output of the 5-bit adder are given at the output as

P5P4P3P2. And the most significant 6th bit is appended with 0 and added with the most significant two bits of the fourth multiplier using 2-Bit adder, the result is given as P7P6 bit of the output.

The total critical path delay is equal to the delay of 3 Full adders and 6 half adders. In the similar manner, we can implement designs of 8*8 and 16*16 multipliers, using four 4*4 and four 8*8 multipliers respectively.

IV. RESULTS AND COMPARISON

We have simulated our design using ModelSim-Altera 6.4a. Coding is done using Verilog. The simulation results of 4*4, 8*8 and 16*16 Multipliers are shown in Fig. 5, Fig. 6, and Fig. 7 respectively. We have synthesized our designs using Xilinx ISE suite 14.3 and obtained the delay using Xilinx Plan Ahead 14.3, the results are shown in TABLE 1.

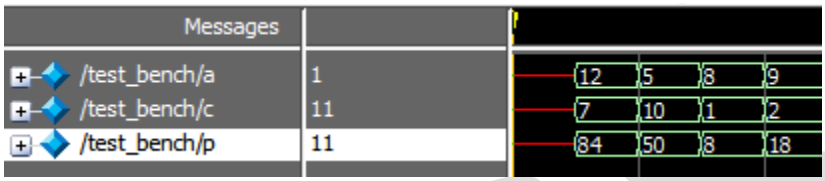


Fig.5. Simulation result of 4*4 Multiplier

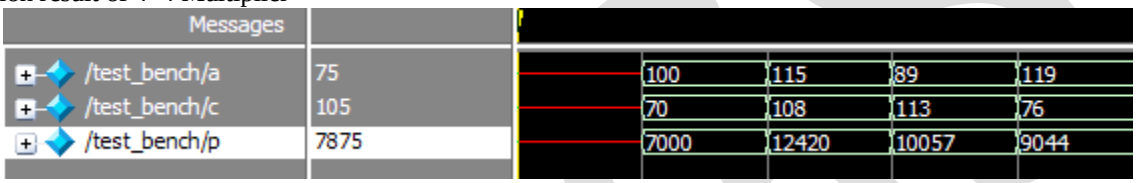


Fig.6. Simulation result of 8*8 Multiplier

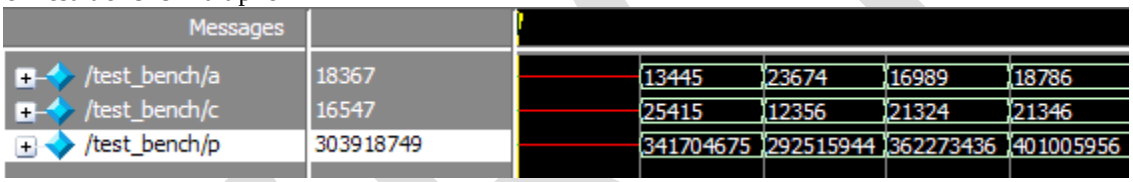


Fig.7. Simulation result of 16*16 Multiplier

Table 1:Synthesis Result of Proposed Design

Device:SPARTAN3: XC3S50:-4	No. of Slices	No. of 4 I/p LUTs	No. of Bonded IOBs	Delay(ns)
4*4	16	29	16	11.695
8*8	84	149	32	18.532
16*16	373	661	64	30.659

We have compared our results with "Modified Booth Wallace Multiplier"[7,10], "High speed Vedic Multiplier" by Ramesh Pushpangadam[10] and "Vedic Mathematics based Multiply Accumulate Unit" by Kabiraj Sethi[7]. The results, as shown in TABLE 2, report that our multiplier design is much faster than other multipliers. Its delay is much less compared to other designs.

Table 2:Comparison of maximum combinational pad to pad delay(ns)

Device:SPARTAN3: XC3S50:-4	Modified Booth Wallace Multiplier[7,10]	Ramesh Pushpangadam[10]	Kabiraj Sethi[7]	Proposed Design
4*4	NA	NA	17.45	11.695
8*8	25.756	25.175	25.06	18.532
16*16	59.238	37.507	36.09	30.659

CONCLUSION

We have designed a multiplier, which is highly efficient in terms of speed. Basic multiplier architecture is based on Vedic Technique and accumulation is done using carry save adder, which gives better performance. On comparison with other multipliers, we have found that our design works with much less delay. For future work, its performance within an ALU can be tested or it can be compared with other Vedic Designs or Conventional Designs

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