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Design of Reconfigurable FFT/IFFT for Wireless Application

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ABSTRACT -— Communication is one of the important aspects of life. The field of communication has seen a fast growth with the advancement in age and with growing demands. Digital domain is now being used for the transfer of signals in place of analog domain. Single – carrier waves are being replaced by multi – carriers for the purpose of better transmission. Multi – carrier systems like CDMA and OFDM are now – a – days being implemented commonly. The orthogonal frequency division multiplexing (OFDM) modulation format has been proposed for variety of digital communications applications such as DVB-T and for wideband wireless communication systems. OFDM requires the use of FFT & IFFT for conversion of signal from time domain to frequency domain and vice versa respectively.

For number of applications the number of FFT/IFFT required changes and so there comes the concept of reconfiguration. This concept of reconfiguration may be used for making the system applicable for various specifications. This paper discuss about the concept of use of reconfigurable FFT in wireless systems to reduce the complexity, cost and power consumption of the system.

Keywords— OFDM, FFT/IFFT, Floating point representation, Complex Multiplier, Reconfigurable FFT/IFFT

INTRODUCTION

OFDM can be seen as either a modulation technique or a multiplexing technique. One of the main reasons to use OFDM is to increase the robustness against frequency selective fading or narrowband interference. Error correction coding can then be used to correct for the few erroneous subcarriers. The concept of using parallel data transmission and frequency division multiplexing was published in the mid-1960s [1, 2]. Some early development is traced back to the 1950s [3]. OFDM has been adopted as a standard for various wireless communication systems such as wireless local area networks, wireless metropolitan area networks, digital audio broadcasting, and digital video broadcasting. It is widely known that OFDM is an attractive technique for achieving high data transmission rate in wireless communication systems and it is robust to the frequency selective fading channels.

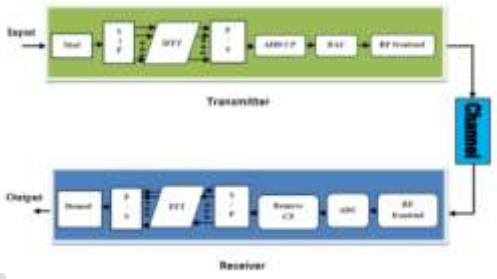


Figure1. A basic diagram of OFDM Transceiver

There are many types of FFT architectures used in OFDM systems. They are mainly categorized into three types namely the parallel architecture, the pipeline architecture and the shared memory architecture. The high performance of a parallel and pipelined architecture is achieved by having more butterfly processing units but they consume larger area than the shared memory architecture. On the other hand, the shared memory architecture requires only one butterfly processing unit and has the advantage of area efficiency.

The rest of the paper is organized as follows. In section II, the FFT algorithm is reviewed. Section III includes comparative study of various methods and architectures available for reconfiguring FFTs for wireless systems. Section IV gives a tabular comparison of the all the methods reviewed. Finally a conclusion is given in section V.

FFT ALGORITHM

Fast Fourier transform (FFT) has been playing an important role in digital signal processing and wireless communication systems. The choice of FFT sizes is decided by different operation standards. It is desirable to make the FFT size changeable according to the operation environment. The Fourier transform is a very useful operator for image or signal processing. Thus it has been extensively studied and the literature about this subject is very rich. The Discrete Fourier Transform (DFT) is used for the digital signal processing and its expression is given below

$$X(k) = \sum_{n=-\infty}^{\infty} x(n) e^{j2\pi \frac{nk}{N}} \quad \text{---(1)}$$

It appears obvious that this expression can not be computed in a finite time due to the infinite bounds. From that, the usully computed expression is the N-points Fast Fourier Transform

Given below

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{j2\pi \frac{nk}{N}} \quad \text{---(2)}$$

The expression of the FFT is bounded and computable with a finite algorithmic complexity.

This complexity is expressed as an order of multiplications and additions. Computing a N-points FFT without any simplification requires an algorithmic complexity of O(N2) multiplications and O(N2) where O denotes the "order of" multiplications and additions. Note that the real number of additions is N(N −1) which is O(N2). This reduction of complexity is however not sufficient for the large FFT sizes that are used in many digital communications standards.

FFT and IFFT methods have three types. One is fixed radix FFT, Mixed radix FFT and Split Radix FFT.[4] Fixed radix decompositions are algorithms in which the same decomposition is applied repeatedly to the OFT equation. The most common decompositions are radix-2, radix-4, radix-8 and radix-16. An algorithm of radix-r can reduce the order of computational complexity to O(N logr(N)). Mixed-radix refers to using a variety of radices in succession. One application of this method is to calculate FFTs of irregular sizes. Mixed-radix can also refer to a computation that uses multiple radices with a common factor. This could be a combination of radices such as 2, 4, and 8. These can be ordered in a way to simplify and optimize calculations of specific sizes or to increase the efficiency of computing FFTs of variable sized inputs. The split-radix algorithm is a method of blending two or more radix sizes and reordering the sequence of operations in order to reduce the number of computations while maintaining accuracy. "Split-radix FFT algorithms assume two or more parallel radix decompositions in every decomposition stage to fully exploit advantage of different fixed-radix FFT algorithms.

FLOATING POINT REPRESENTATION

Floating point numbers are one possible way of representing real numbers in binary format; the IEEE 754 standard presents two different floating point formats, Binary interchange format and Decimal interchange format. Fig. 2 shows the IEEE 754 single precision binary format representation; it consists of a one bit sign (S), an eight bit exponent (E), and a twenty three bit fraction (M or Mantissa). [5]If the exponent is greater than 0 and smaller than 255, and there is 1 in the MSB of the significand then the number is said to be a normalized number; in this case the real number is represented by

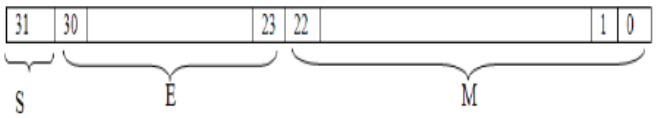


Figure 2. IEEE single precision floating point format

Sign Bit: This bit represents whether the number is positive or negative. 0 denotes a positive number and 1 denotes a negative number.

Exponent: This field represents both positive and negative exponents. This is done by adding a bias to the actual exponent in order to get the stored exponent. For IEEE 754 this value is 127.

Mantissa: This field is also known as the significant and represents the precision bits of the number. It comprises of implicit leading bits and the fraction bits.

Table I

Precision	Sign	Exponent	Fraction	Bias
Single Precision	1[32]	8 [30-23]	23 [22-00]	127
Double Precision	1 [63]	11 [62-52]	52 [51-00]	1023

In proposed work, the BCD input is first converted into floating number format. The process of addition, subtraction and multiplication in the middle stage i.e. the complex multiplier takes place in floating point format only.

At the end the floating output is again converted into BCD. The system can process signed, unsigned and decimal numbers thereby increasing the range.

Reconfigurable architecture

A Reconfigurable FFT Architecture can be implemented by cascading several radix-2 stages in order to accommodate different FFT sizes. The signal-flow graphs for radix-2 to radix- 24 butterflies are shown in Fig. 3

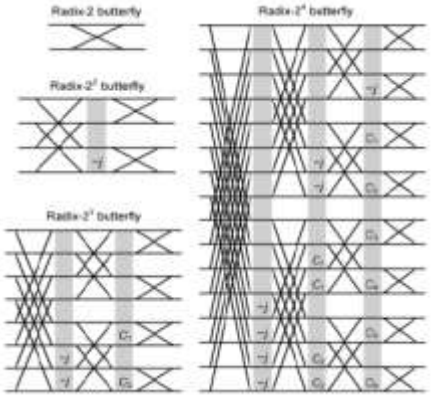


Fig. 3 Various Butterfly Operations

Radix-2

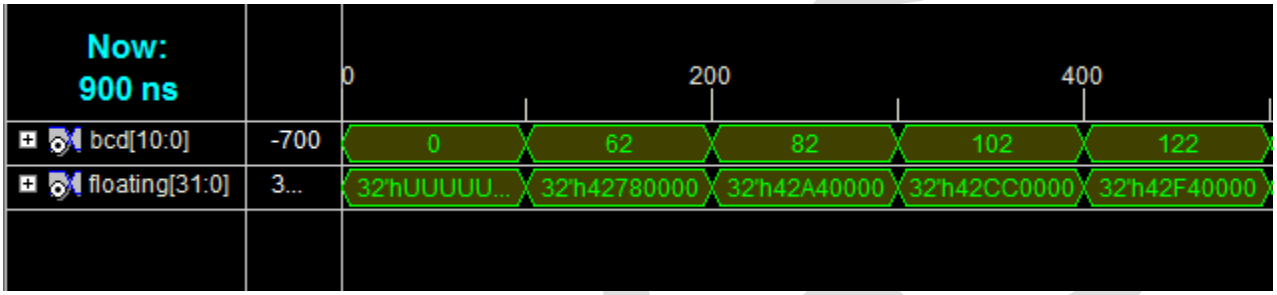
The radix-2 PE applies one stage of radix-2 butterfly computations to its data. It is used when the size of the frame to be processed is 32 or 128 points. [7]The radix-2 PE is realized as a simplified radix-4 PE (Figure 2). The Butterfly Core is replaced with the simpler radix-2 butterfly network, consisting of two (2) complex adders/subtractors and one (1) complex multiplier. This circuit though is optimized further. In the split radix 128 and 32 point FFT computation, the twiddle factors for all radix- 2 butterflies have the constant value of (1+0j). Plugging into the radix-2 butterfly equations we obtain:

Consequently, the complex multiplier (in the butterfly core) and the twiddle generator blocks are omitted.

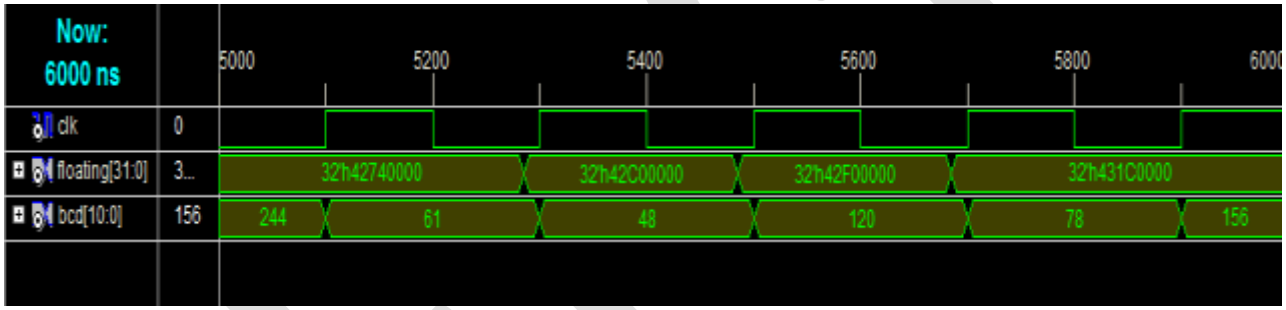
The general fixed-radix algorithms decompose the FFT by letting r=rl=r2...=rm. The r-point DFT is called the butterfly, which is a basic operation unit. Higher radix decomposition is often preferred because it can reduce the computational complexity by reducing the number of complex multiplications required. The trade-off is that the hardware complexity of the butterfly grows as the radix becomes high. However, a fixed-radix algorithm is sometimes found deficient due to its limitation on FFT size (power of r). As we prefer higher radix algorithms to reduce the computational complexity, the flexibility of the FFT size is also limited. Therefore, the mixed-radix algorithm is adopted in our design to keep the architecture flexible while using a high radix algorithm.

SIMULATION RESULTS

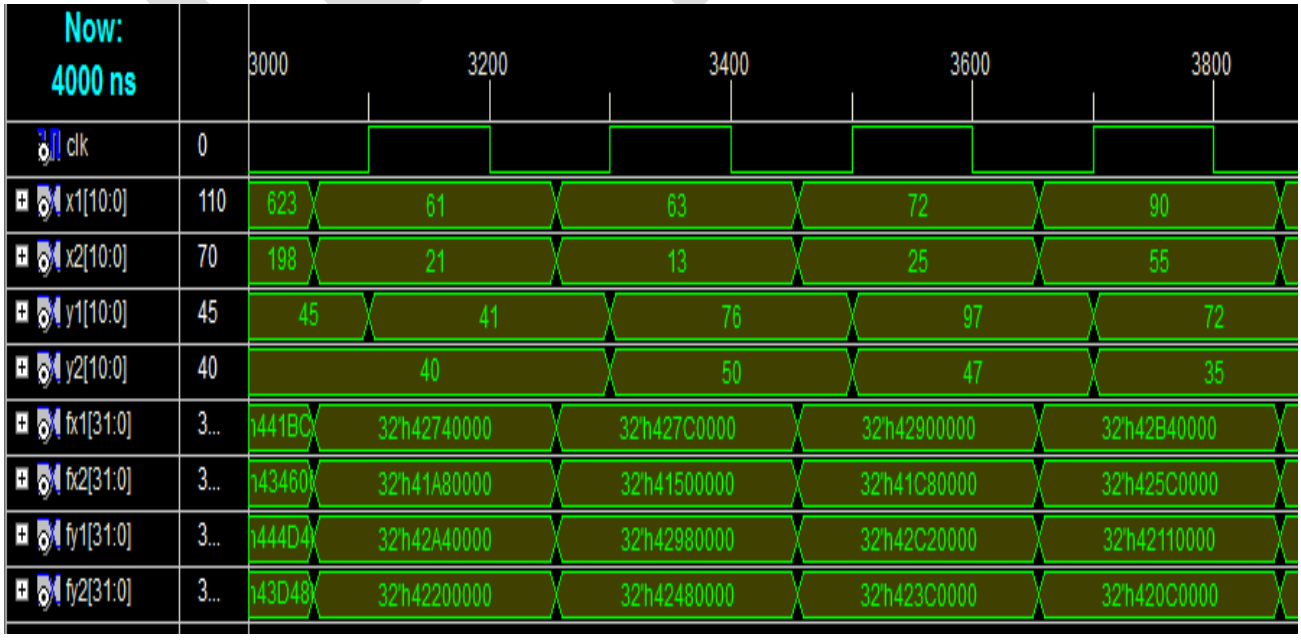
1. BCD to Floating Point Representation:



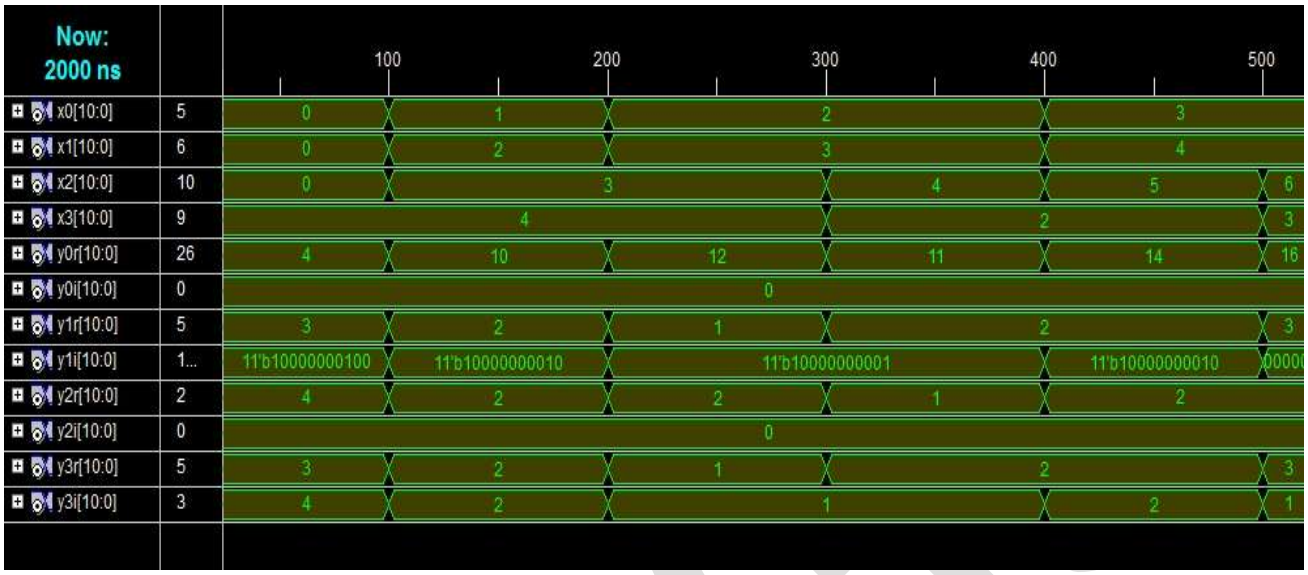
2. FLOATING POINT REPRESENTATION TO BCD:



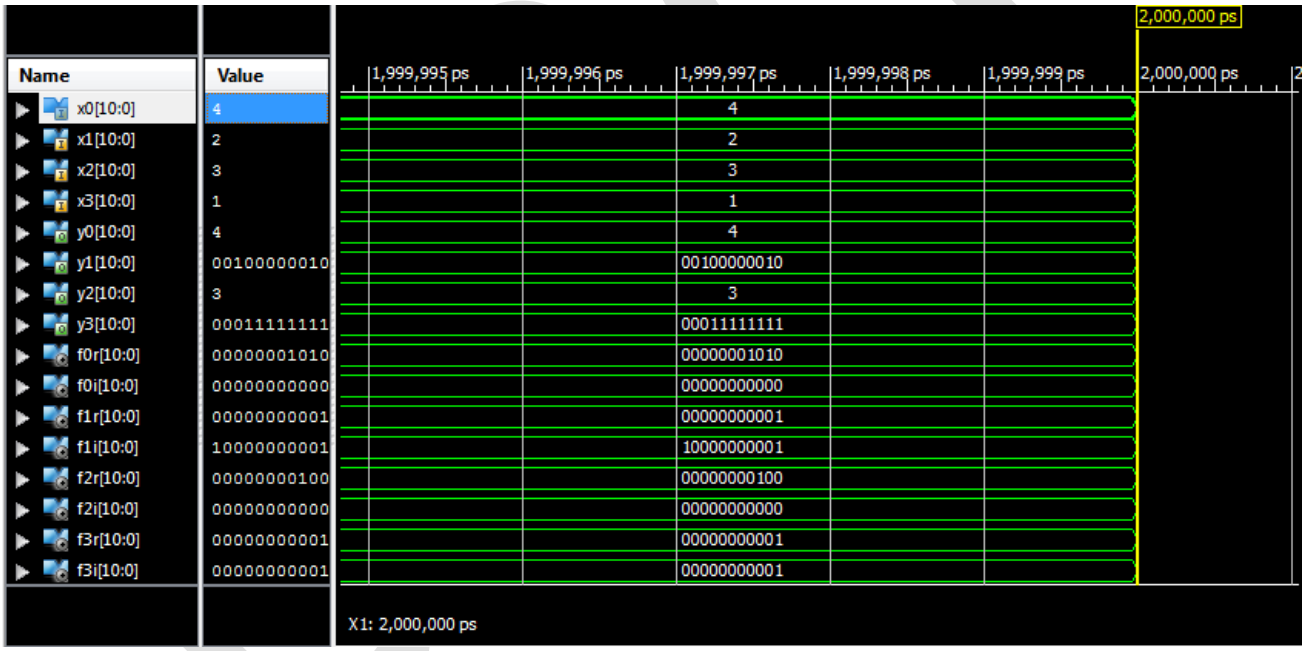
3. 2- POINT FFT:



4. 4-POINT FFT:



5. 4-POINT IFFT



CONCLUSIONS

This paper presents various methods for programmable FFT/IFFT processor design has been for OFDM applications. The paper includes various low power, reduced complexity, and low cost methods of reconfigurable FFT/IFFT. The method used shows that by making use of floating point format the FFT/IFFT of signed, unsigned, decimal numbers can be obtained efficiently. Also by making use of reconfigurable architecture the system itself can be capable of switching into the radix algorithm according to the provided input and can provide the correct computation result. Using vedic mathematics for the complex computation helps to increase the speed of the computations and provide efficient results.

REFERENCES:

[1] BaigI,Jeoti V 'DCTprecoded SLM technique for PAPR Reduction' Intelligent and Advanced System international Conference,15-17 June 2010.
[2] S.P.Vimal ,K.R.Shankar Kumar 'A New SLM Technique for PAPR Reduction in OFDM Systems', European Journal for scientific Research ISSN 1450-216X vol.65,No.2,2011.
[3] OFDM Simulation using Matlab 'Smart Research Laboratory'faculty advisor Dr.Mary Ann Ingram ,Guillermo Acosta ,Aug2000.
[4] Md Nooruzzaman Khan M.Mohamed Ismail Dr.P .K.J awahar II M.Tech(VLSI & Embedded Systems) Associate Professor Professor "An Efficient FFT IIFFT Architecture for Wireless communication" ICCSP-'12
[5] Preethi Sudha Gollamudi, M. Kamaraju Dept. of Electronics & Communications Engineering Gudlavalleru Engineering College, Andhra Pradesh, India-769008 "Design Of High Performance IEEE- 754 Single Precision (32 bit) Floating Point Adder Using VHDL" International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 7, July – 2013 IJERTIJERT ISSN.
[6] Sharon Thomas & 2V Sarada 1 Dept. of VLSI Design, 2Department of ECE, 1&2 SRM University " Design of Reconfigurable FFT Processor With Reduced Area And Power "ISSN (PRINT) : 2320 – 8945, Volume -1, Issue -4, 2013
[7] Konstantinos E. MANOLOPOULOS, Konstantinos G. NAKOS, Dionysios I. REISIS and Nikolaos G. VLASSOPOULOS Electronics Laboratory, Department of Physics National and Capodistrian University of Athens "Reconfigurable Fast Fourier Transform Architecture for Orthogonal Frequency Division Multiplexing Systems"
[8] Anuj Kumar Varshney 1, Vrinda Gupta 2 Department of Electronics and Communication Engineering .National Institute of Technology, Kurukshetra, Haryana Kurukshetra 136119, India "Power-Time Efficient Algorithm for Computing Reconfigurable FFT in Wireless Sensor Network" International Journal of Computer Science & Engineering Technology (IJCSET)

SPNA071A–November 2006 Implementing Radix-2.